



UNITED STATES PATENT AND TRADEMARK OFFICE

11A
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,340	03/17/2004	Thomas Nulsen	NPT-65.0402	5585

7590 01/24/2007
Wagner, Murabito & Hao LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER

NGUYEN, HIEP

ART UNIT	PAPER NUMBER
----------	--------------

2816

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/803,340

Applicant(s)

NULSEN ET AL.

Examiner

Hiep Nguyen

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 November 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 10-14 and 18-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-14 is/are allowed.
- 6) ☒ Claim(s) 1, 4, 5 and 18 is/are rejected.
- 7) ☒ Claim(s) 2, 3, 19 and 20 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input checked="" type="checkbox"/> Other: <u>attached drawing</u> . |

DETAILED ACTION

This is responsive to the amendment filed on 11-16-06. Applicant's arguments with respect to reference Yamamoto (US. 5,444,744) have been carefully considered but they are not deemed to be persuasive to overcome the reference. Thus, the claims remain rejected under Yamamoto. The rejection changes slightly for clarification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, 5 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamamoto et al. (USP. 5,444,744).

Regarding claim 1, figures 8 and 10A-10I of Yamamoto show a clock based voltage deviation detector comprising:

a pulse module (15b) having a pulse input for receiving a clock signal (J) and a pulse output for outputting a stream of reset pulses (B);

an indicator module (9a, 11, 12, 21) having a first indicator input for receiving an input signal (I4), a second indicator input for receiving a reference voltage (9b), a third indicator input communicatively coupled to said pulse output (B) of said pulse module (15b) and an indicator output for outputting a pass/fail indicator signal (I) as a function of said stream of reset pulses (B) and a difference between an input signal (I4) and a reference voltage (9b), and

a correlation module (23, 24, 22, 25) having a first correlation input for receiving said clock signal (J), a second correlation input communicatively coupled to said indicator output of said indicator module, wherein an event of said pass/fail indicator is correlated to a period of said clock signal at which said event occurred.

Regarding claim 4, the indicator module comprises:

Art Unit: 2816

a comparator (9a) having a first comparator input for receiving input signal (I4), a second comparator input for receiving reference voltage (9b) and a comparator output for outputting a trip signal (K) as a function of a difference between said input signal and said reference; and

a latch (11) having a first input communicatively coupled to the comparator output of the comparator, a second input communicatively coupled to pulse output (B) and a latch output for outputting the pass/fail indicator (K) as a function of said trip signal (K) and said stream of reset pulses (B).

Regarding claim 5, figure 8 of Yamamoto shows a latch enable comparator (9a, 11) having first to third inputs receiving input signal (I4), reference voltage (9b) and pulse output (B) of the pulse module (15b).

Regarding claim 18, figure 8 shows a clock based voltage deviation detector comprising:

a means for generating a reset pulse stream as a function of a clock signal (15b);

a means for generating a pass/fail indicator signal as a function of said reset pulse stream and an event of a monitored voltage (9a, 11, 12, 21); and

a means for correlating an event of said pass/fail indicator signal with a specific period of said clock signal at which said event occurred (23, 24, 22, 25).

Allowable Subject Matter

Claims 10-14 are allowed because the prior art (US. 5,444,744) fails to teach or suggest a clock based voltage deviation detector comprising a counter and a storage module.

Claims 2, 3, 19 and 20 are objected to because the prior art fails to teach or suggest a pulse module comprising a delay cell and an exclusive-OR gate as called for in claim 2; a correlation module comprising a counter and a storage module; clock based voltage deviation detector comprising a means for generating a reset pulse stream and a means for further generating the pass/fail indicator signal as called for in claim 19.

Response to Arguments

It appears that, in the Remarks, the Applicant relies on the labels to distinguish the application from the prior art. In claim 1, the Applicant only recites “ pulse module having a pulse input for receiving a clock signal and a pulse output for outputting a stream of reset pulses... for outputting a pass/fail indicator signal as a function of said stream of reset pulses”. The recitation “ a stream of reset pulses” is merely a label that does not have any specific function thus, any stream of signal can be considered as a stream of reset pulses. In page 4 of the Remarks, the Applicant argues that “ Yamamoto fails to teach or fairly suggest "a pass/fail indicator signal as a function of said stream of reset pulses and a difference between an input signal and a reference voltage" as recited by Claim 1. Even if, arguendo, signal "B" can be construed as the recited stream of reset pulses, there is no signal illustrated in Yamamoto that teaches or fairly suggests the recited "pass/fail indicator signal." Figure 8 of Yamamoto shows the indicator module (9a, 11, 12, 21) receiving an input signal (I4), a reference voltage (9b) and a stream of reset pulses (B). The correlation module (23, 24, 22, 25) having a first correlation input for receiving clock signal (J), a second correlation input communicatively coupled to indicator output (D) which is a function of input signal (I4) and reference voltage (9b) of the indicator module. Therefore, the “pass/fail indicator signal” (I) is a function of input signal (I4), reference voltage (9b) of the indicator module and the stream of reset pulses (B)”. Moreover, the recitation “pass/fail indicator signal” is just a label. The difference between the input signal (I4) and the reference voltage (9b) is generated by amplifier (9a).

Conclusion

Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to

Art Unit: 2816

37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

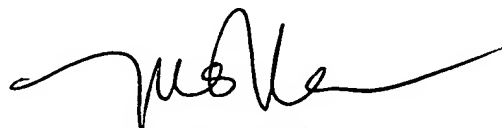
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

01-18-06



TUANT.LAM
PRIMARY EXAMINER

